WE CLAIM:

1. An apparatus for generating a pulsed output signal, comprising:

a comparator circuit that is configured to receive a ramp signal, a selected signal, and a comparator reset signal, wherein an output associated with the comparator circuit is maintained in a reset condition when the comparator reset signal is asserted, and wherein the comparator circuit is arranged to selectively assert a comparison signal in response to the selected signal and the ramp signal when the comparator reset signal is de-asserted;

a signal selector circuit that is configured to receive a first signal, a second signal, and a selector control signal, wherein the signal selector circuit is arranged to select the first signal as the selected signal when the selector control signal is de-asserted, and wherein the signal selector circuit is arranged to select the second signal as the selected signal when the selector control signal is asserted; and

a logic circuit that is configured to receive a clock signal and the comparison signal, wherein the logic circuit is arranged to: de-assert the selector control signal when the clock signal is asserted, assert the selector control signal when the clock signal is de-asserted and the comparison signal is asserted, de-assert the pulse output signal when the clock signal is asserted, assert the comparator reset signal when the clock signal is asserted, assert the pulsed output signal while the clock signal is de-asserted and the ramp signal is between the first signal and the second signal.

2. The apparatus of Claim 1, wherein the signal selector circuit is a multiplexer that is arranged to selectively couple one of the first and second signals to the comparator circuit in response to the selector control signal.

3. The apparatus of Claim 1, the logic circuit comprising: a latch circuit that includes a reset terminal, a set terminal, and an output terminal, wherein the set terminal is coupled to the clock signal, the reset terminal is coupled to the comparison signal, and the output terminal is arranged to provide the selector control signal.

4. The apparatus of Claim 1, the logic circuit comprising: a flip-flop circuit that includes a D-input terminal, a clock terminal, a reset terminal, and an output terminal, wherein the D-input terminal is coupled to a power signal, the clock terminal is coupled to the selector control signal, the reset terminal is coupled to the clock signal, and the output terminal is arranged to provide the pulsed output signal.

5. The apparatus of Claim 1, the logic circuit comprising: a latch circuit, wherein the latch circuit is arranged to assert an enable reset path signal when the comparison signal is de-asserted and the selector control signal is asserted, wherein the latch circuit is arranged to de-assert the enable reset path signal when the selector control signal is de-asserted, wherein the comparator reset signal is asserted when the enable reset path signal is de-asserted and the selector control signal is asserted, and wherein the pulsed output signal is de-asserted when the enable reset path signal is asserted and the comparison signal is asserted.

6. The apparatus of Claim 1, the logic circuit further comprising: a first logic circuit and a second logic circuit, wherein the first logic circuit is arranged to assert the reset comparator signal in response to the clock signal, wherein the first logic circuit is also arranged to assert the reset comparator signal when the enable reset path signal is asserted and the selector control signal is asserted, wherein the second logic circuit is arranged to assert the enable reset path signal when the comparison signal is de-asserted and the selector control signal is asserted, wherein the second logic circuit is arranged to de-assert the enable reset path signal when the selector control signal is de-asserted.

7. The apparatus of Claim 6, the logic circuit further comprising: a third logic circuit, wherein the third logic circuit is arranged to de-assert the pulsed output signal when the enable reset path signal is asserted and the comparison signal is asserted, and wherein the third logic circuit is also arranged to de-assert the pulsed output signal when the clock signal is asserted.

8. The apparatus of Claim 7, the logic circuit further comprising: a fourth logic circuit and a fifth logic circuit, wherein the fourth logic circuit is arranged to assert the selector control signal when the comparison signal is asserted, and de-assert the selector control signal when the clock signal is asserted, and wherein the fifth logic circuit is arranged to assert the pulsed output signal when the selector control signal transitions from de-asserted to asserted.

9. A method for providing a pulsed output signal, comprising:

selecting a first operating mode while a clock signal is asserted;

de-asserting the pulsed output signal during the first operating mode;

selecting a second operating mode when the clock signal is de-asserted during the first operating mode;

comparing a ramp signal to a first signal during the second operating mode;

selecting a third operating mode when the ramp signal exceeds the first signal during the second operating mode;

comparing the ramp signal to a second signal during the third operating mode, wherein the second signal is different from the first signal; and

asserting the pulsed output signal during the third operating mode while the second signal is greater than the ramp signal.

10. The method of Claim 9, wherein selecting a first operating mode includes: resetting a comparator circuit, and coupling the first signal to the comparator circuit.

11. The method of Claim 9, wherein selecting a second operating mode includes: enabling a comparator circuit, and starting the ramp signal.

12. The method of Claim 9, wherein selecting a third operating mode includes: coupling the second signal to the comparator circuit.

13. The method of claim 9, further comprising: disabling a reset path when the first operating mode is selected, enabling the reset path when the third operating mode is selected, wherein pulsed output signal is set as asserted when the ramp signal exceeds the first signal in the second operating mode, and wherein the pulsed output signal is reset when the reset path is enabled and the ramp signal exceeds the second signal in the third operating mode.

14. The method of claim 9, wherein the pulsed output signal is asserted in the second operating mode when the ramp signal exceeds the first signal by an amount, wherein the pulsed output signal is de-asserted in the third operating mode when the ramp signal exceeds the second signal by the amount, wherein the amount is associated with a systematic error in the comparison, and wherein the pulse width is relatively unaffected by the systematic error.

15. An apparatus for providing a pulsed output signal, comprising:

a means for comparing, wherein the means for comparing is arranged to compare a selected signal to a ramp signal to provide a comparison signal;

a means for activating an operating mode, wherein a first operating mode is activated when a clock signal is asserted, a second operating mode is activated when the clock signal is de-asserted during the first operating mode, and a third operating mode is activated when the comparison signal is asserted during the second operating mode;

a means for selecting, wherein the means for selecting is arranged to select a first signal when the first operating mode is activated, and wherein the means for selecting is arranged to select a second signal when the third operating mode is activated, wherein the first signal and the second signal are different from one another by an amount that is related to a pulse width;

a means for setting the pulsed output signal when the third operating mode is activated;

a first means for resetting, wherein the first means for resetting is arranged to reset the means for comparing when the comparison signal is asserted during the second operating mode;

a second means for resetting, wherein the second means for resetting is arranged to reset the means for comparing during the first operating mode;

a third means for resetting, wherein the third means for resetting is arranged to reset the pulsed output signal when the comparison signal is asserted during the third operating mode; and

a fourth means for resetting, wherein the fourth means for resetting is arranged to reset the pulsed output signal when the first operating mode is activated.

16. An apparatus as in Claim 15, further comprising: a means for initiating, wherein the means for initiating is arranged to start the ramp signal when the second operating mode is activated.

17. An apparatus as in Claim 15, further comprising: a means for disabling a reset path when the first operating mode is activated, a means for enabling the reset path when the third operating mode is activated, wherein the third means for resetting is disabled when the reset path is disabled.

18. An apparatus as in Claim 15, wherein the comparison signal is asserted when the ramp signal exceeds the first signal by a first amount during the second operating mode.

19. An apparatus as in Claim 18, wherein the comparison signal is asserted when the ramp signal exceeds the second signal by a second amount during the third operating mode, wherein the first amount and the second amount are approximately the same as one another such that an accurate pulse width is maintained.

20. An apparatus as in Claim 15, further comprising a feedback means that is arranged to provide the second signal in response to the pulsed output signal.